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(54) Crystal-axis-aligned vertical side wall DRAM and process for manufacture thereof

(57) A dynamic random access memory (DRAM) cell comprising a deep trench storage capacitor having an active transistor device partially disposed on a side wall of the trench. The side wall is aligned to a first crystallographic plane having a crystallographic orientation along a single crystal axis. A process for manufacturing such a DRAM cell comprises: (a) forming a deep trench in a substrate, (b) forming a faceted crystal region along the trench side wall having a single crystallographic orientation, and (c) forming a transistor device partially disposed on the faceted crystal region in the side wall. The faceted crystal region may be formed by growing an oxide collar, such as by local thermal oxidation under oxidation conditions selected to promote a higher oxidation rate along a first family of crystallographic axes than along a second family of crystallographic axes.

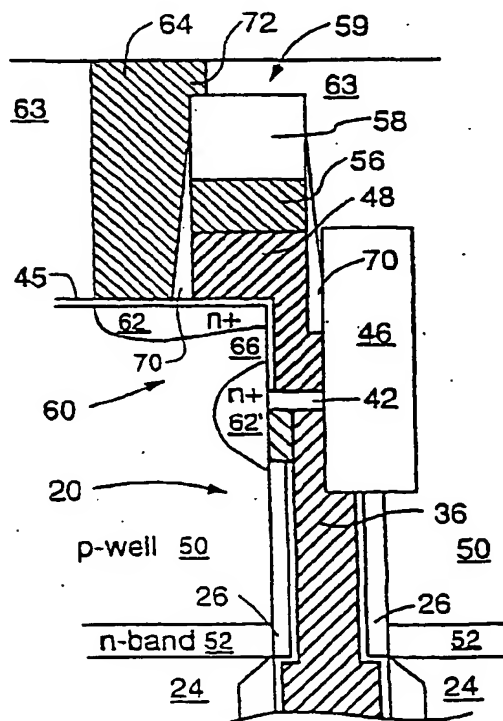


Fig. 12

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Description

TECHNICAL FIELD

[0001] The present invention relates generally to semiconductor transistor devices and, more specifically, to DRAM cells having non-planar transistor channel regions.

BACKGROUND OF THE INVENTION

[0002] Dynamic Random Access Memory (DRAM) cells can retain information only temporarily, on the order of milliseconds, even with power continuously applied. Therefore, the cells must be read and refreshed at periodic intervals. Although the storage time may appear to be short, it is actually long enough to allow many memory operations to occur between refresh cycles. The advantages of cost per bit, device density, and flexibility of use (i.e., both read and write operations are possible) have made DRAM cells the most widely used form of semiconductor memory to date. The earliest DRAM cells were three-transistor cells. Today, DRAM cells consisting of only one transistor and one capacitor have been implemented.

[0003] As DRAM circuits are scaled to small dimensions, it becomes increasingly important to form compact array cell layouts. The active device transistor is placed along the vertical side wall of a deep-trench storage capacitor in one type of array cell layout. Such a configuration forms a non-planar transistor device.

[0004] The non-planar transistor channel region crystal orientation can be a function of lithographic-projected image shape and the overlay between lithographically defined deep trench and active area patterns. Gate oxide thickness, surface state density, and other physical and electrical properties may be a function of the projected image shape and the overlap between the deep trench and active area patterns. These physical and electrical properties influence the transistor electrical, physical, and reliability characteristics.

[0005] As shown in Fig. 1, a typical deep trench having an elliptical cross section has a vertical side wall 32 that cuts across a continuum of planes including {001} and {011} crystal planes. Side wall 32 is not aligned with any particular crystal plane. Therefore, side wall 32 has associated crystal-plane-dependent properties that vary as side wall 32 makes a curved transition from one crystallographic plane to the other.

[0006] In accordance with standard crystallographic nomenclature, various symbols have specified meanings. Among those symbols are rounded brackets, {}, which refer to families of equivalent crystallographic planes (i.e., the {001} family of planes); parentheses, (), which refer to specific crystallographic planes (i.e., the (100) plane); horizontal triangles, <>, which refer to families of equivalent crystallographic axes (i.e., the <011> family of axes); and square brackets, [], which refer to

a specific crystal axis (i.e., the [110] axis). For example, in silicon crystals, the (100) plane and the (001) plane are equivalent to one another and, thus, are both in the same {001} family of planes.

[0007] For optimized device performance, it is desirable to provide a side wall device aligned to a single crystallographic plane having a crystallographic orientation along a single crystal axis. It is an object of the present invention, therefore, to provide a crystal-axis-aligned, non-planar transistor structure. A related object is to provide a process for obtaining such a structure.

SUMMARY OF THE INVENTION

[0008] To achieve these and other objects, and in view of its purposes, the present invention provides a dynamic random access memory (DRAM) cell. The cell comprises a deep trench storage capacitor having an active transistor device partially disposed on a side wall of the deep trench. The side wall is aligned to a first crystallographic plane having a crystallographic orientation along a single crystal axis. The substrate surface may be aligned along a second crystallographic plane. The first and second crystallographic planes may be in the same family of equivalent crystallographic planes, such as the {001} family, or the first and second crystallographic planes may be in different families.

[0009] The present invention also provides a process for manufacturing a DRAM cell. The process comprises: (a) forming a deep trench in a substrate, (b) forming a faceted crystal region having a single crystallographic orientation along the trench side wall, and (c) forming a transistor device partially disposed on the faceted crystal region in the side wall. The faceted crystal region may be formed by growing an oxide collar, such as by local thermal oxidation under oxidation conditions selected to promote a higher oxidation rate along a first family of crystallographic axes, such as along the <011> family of crystal axes, than along a second family of crystallographic axes, such as along the <100> family of crystal axes. Other chemical and physical mechanisms may also be used to induce faceting in the trench side wall.

[0010] It is to be understood that both the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the invention.

BRIEF DESCRIPTION OF THE DRAWING

[0011] The invention is best understood from the following detailed description when read in connection with the accompanying drawing. It is emphasized that, according to common practice, the various features of the drawing are not to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Included in the drawing are the following figures:

Fig. 1 is a schematic illustration plan view of an exemplary deep trench structure having crystal orientations as shown;

Fig. 2 is a schematic illustration plan view of the deep trench structure of Fig. 1 after a local oxidation step, highlighting the faceted side walls of the trench according to the present invention;

Fig. 3 is a schematic, cross-sectional illustration of the trench of Fig. 1 taken along the line 3-3;

Figs. 4 through 10 are schematic, cross-sectional, in-process illustrations of the trench of Fig. 2 taken along the line 4-4 depicting steps in an exemplary process for manufacturing an exemplary DRAM cell of the present invention, with Fig. 4 showing an isolation collar formed in the upper region of the trench and a buried plate in the lower region of the trench;

Fig. 5 shows the trench of Fig. 4 after a dielectric is applied and the trench is partly filled with polysilicon;

Fig. 6 shows the trench of Fig. 5 after the collar is etched;

Fig. 7 shows the trench of Fig. 6 after a buried strap is formed;

Fig. 8 shows the trench of Fig. 7 after the buried strap is removed from the side walls of the trench above the polysilicon and above the pad;

Fig. 9 shows the trench of Fig. 8 after a trench-top dielectric is formed, the pad is stripped, a sacrificial oxide is grown on the exposed surface of the substrate and on the exposed side wall of the trench, a p-well and an n-band are created in the substrate, and diffusion regions are formed in the substrate;

Fig. 10 shows the trench of Fig. 9 after the sacrificial oxide is removed, a gate oxide is grown, a conductive gate layer is formed, an active area is patterned, an etching step is performed to etch shallow trench isolation (STI) regions everywhere except in the active area, the STI regions are filled and planarized to the pad nitride, and the pad nitride is stripped away;

Fig. 11A is a schematic illustration plan view of an exemplary DRAM cell, made according to the present invention, with the device-oriented along a crystallographic plane in the same family as the substrate surface;

Fig. 11B is a schematic illustration plan view of an exemplary DRAM cell, made according to the

present invention, with the device oriented along a different crystallographic plane in a different family from the substrate surface; and

Fig. 12 is a schematic cross-sectional illustration of the DRAM cell of Fig. 11A or Fig. 11B taken along the line 12-12.

DETAILED DESCRIPTION OF THE INVENTION

[0012] Referring now to the drawing, in which like reference numbers refer to like elements throughout, Figs. 1-12 show various aspects of an exemplary DRAM cell of the present invention and intermediate steps in the process for making the cell. As shown in Figs. 1 and 3, a typical deep trench storage capacitor 10 is formed into a pad 22 and a substrate 24 by conventional processing techniques well known in the art. For example, an optical lithography step may be used to form a pattern on pad 22. Then a dry etching step, such as reactive-ion etching (RIE), may be used to create a trench 20 to a desired depth through pad 22 and into substrate 24.

[0013] The cross-sectional pattern of deep trench 20 is typically an ellipse that cuts across crystal axes A and B. For example, as shown in Fig. 1, axis A may have a [011] crystallographic orientation and axis B may have a [001] orientation. Substrate 24 is typically silicon and pad 22 is typically a silicon nitride (SiN) layer having a thickness of about 10 nm to about 100 nm. There may also be a thin thermal oxide layer (not shown), typically about 3 nm to about 10 nm thick, between substrate 24 and pad 22. Deep trench 20 generally has a depth of about 3 μ m to about 10 μ m and a diameter or maximum width that is a function of the lithographic ground rule, typically about 0.5 μ m to less than 0.1 μ m. Trench 20 has side walls 32 and a bottom 33.

[0014] As shown in Figs. 2 and 4, in accordance with the present invention, an isolation collar 26 is formed in upper region 28 of trench 20. Upper region 28 typically comprises 10 to 20% of the total depth of trench 20. Collar 26 may be formed using local thermal oxidation (LOCOS), such as by the exemplary process explained below, or by other physical and chemical mechanisms, as also indicated below.

[0015] Before the oxidation step, a barrier film (not shown) may be formed along the exposed surfaces of trench 20 and pad 22 such as by a low-pressure chemical vapor deposition (LPCVD) of a SiN film having a thickness of about 2 nm to about 10 nm. The barrier film is then removed from upper region 28, for example by filling trench 20 with photoresist (not shown) and partially etching the photoresist down into trench 20 to a depth controlled by the amount of overetch time. This step exposes the barrier film in upper region 28 while leaving the lower region 30 covered. The exposed barrier film may then be removed in upper region 28 of trench 20 and from pad layer 22, for example, by chemical or dry etching, and then the photoresist stripped away. Other

processes for isolating side wall 32 in upper region 28 while protecting side wall 32 in lower region 30 may also be used.

[0016] The local oxidation step is then performed at oxidation conditions that promote the oxidation rate along one family of crystal axes over another, such as, for example, promoting oxidation along $\langle 001 \rangle$ axes over $\langle 001 \rangle$ axes. For instance, the oxidation step may comprise the use of oxygen (O_2) or water (H_2O) at a temperature of between about $800^\circ C$ and about $1,100^\circ C$ for between about 2 minutes and about 10 minutes, not including ramping time, to achieve an oxide isolation collar 26 having a thickness of between about 10 nm to about 50 nm. Such oxidation conditions induce faceting of the underlying silicon substrate 24 during growth of collar 26.

[0017] Thus, the curved trench wall 32 having an elliptical cross section, as shown in Fig. 1, facets into a polygonal cross section having distinct planar walls 32' and 32" aligned with crystal planes (001) and (011), respectively, as shown in Fig. 2. Faceted walls 32' and 32" thus have consistent physical and electrical properties along the faceted structure, providing improved transistor electrical, physical, and reliability characteristics as compared to transistors built on unfaceted trench walls. The thermal oxide collar 26 and associated faceting are formed only on side walls 32 in upper region 28 of trench 20; the barrier film protects side walls 32 in lower region 30 of trench 20.

[0018] Faceted side walls 32', 32" may be formed, as described above, by thermal oxidation. Faceted side walls 32', 32" may instead be formed by other physical or chemical mechanisms. Such mechanisms include, for example, preferential crystal axis etching, such as etching with potassium hydroxide (KOH), as is well-known in the art.

[0019] The remaining DRAM structure may be constructed according to processes well known in the art, such as the exemplary process described below. The process provided below is not intended to be a limitation of the present invention, but rather is included for illustration. In such an exemplary process, the barrier film in lower region 30 is stripped via a process that selectively leaves thermal oxide isolation collar 26 in upper region 28 of trench 20. Buried plate 34 is then created in lower region 30, leaving the configuration shown in Fig. 4. Buried plate 34 may be created by doping lower region 30 of trench 20 to form an out-diffusion in substrate 24 using collar 26 as a mask for upper region 28. The out-diffusion may be formed using arsenosilicate glass (ASG) drive-in, plasma doping (PLAD), plasma ion implantation (PIII), gas-phase diffusion of arsenic (As) or phosphorus (P), or other techniques known in the art.

[0020] Next, as shown in Fig. 5, a thin node dielectric 35 is created, such as by thermal nitridation, for example with ammonia (NH_3), followed by LPCVD of SiN. Finally, trench 20 is filled, such as with an n+ doped LPCVD polysilicon 36, and recessed to a desired depth D1.

Depth D1 is typically about 300 nm to about 700 nm, preferably between 300 to 450 nm.

[0021] Isolation collar 26 is then etched away, such as with a wet etch using a solution containing hydrogen fluoride (HF), to expose side walls 32 in the area where the collar 26 is not covered by polysilicon 36 and below the polysilicon level to a depth D2, as shown in Fig. 6. D2 is typically about 10 nm to about 50 nm.

[0022] Next, as shown in Fig. 7, a buried strap 40 is formed. Typically of LPCVD silicon, buried strap 40 is formed in a layer having a thickness of about 10 nm to about 50 nm. As shown in Fig. 8, buried strap 40 is then removed from side walls 32 of trench 20 above polysilicon 36 and above pad 22, such as by an isotropic wet chemical or dry etching step.

[0023] Then, as shown in Fig. 9, trench-top dielectric 42 or trench-top oxide (TTO) is formed, such as by an anisotropic high-density plasma (HDP) or other bias-assisted oxide deposition step. The creation of trench-top dielectric 42 typically forms a corresponding layer (not shown) atop pad 22, which is removed by a chemical mechanical polishing (CMP) step as is known in the art. Thus exposed, pad 22 is then stripped, typically by a wet chemical etch step selective to trench-top dielectric 42, and a sacrificial oxide 44 is grown on the exposed surface of substrate 24 and exposed side wall 32 of trench 20, as shown in Fig. 9.

[0024] Ion implantation may then be used to create a p-well 50 and an n-band 52 below p-well 50 in substrate 24. Similarly, ion implantation of As or P may be used to create diffusion region 62. Another diffusion region 62' is created by out-diffusion from n+ doped polysilicon region 36 through buried strap 40. Such process steps yield the structure shown in Fig. 9. Other device-threshold-tailoring implants may also be created at this time.

[0025] Next, as shown in Fig. 10, sacrificial oxide 44 is removed, such as by a chemical wet etch process with an HF-containing solution. Then, gate oxide 45 is grown and a conductive gate layer 48, such as polysilicon having a thickness approximately equal to the diameter of trench 20, is formed. A nitride pad (not shown) is formed having a thickness of approximately half to approximately equal to the thickness of gate layer 48.

[0026] An active area 54 is patterned (see Figs. 11A and 11B), typically by photolithography, and an etching step, such as RIE, is performed to etch shallow trench isolation (STI) regions 46 everywhere except in active area 54. STI regions 46 are filled, typically with an oxide, and planarized by a CMP step down to the pad nitride. The pad nitride is then stripped away, leaving the structure shown in Fig. 10.

[0027] Next, a thin seed layer of polysilicon is typically deposited, extending polysilicon gate layer 48 over the edge of trench 20 and over top diffusion region 62 in p-well 50 of substrate 24. Middle layer 56, which typically comprises a higher conductivity material than polysilicon gate layer 48, such as tungsten (W) or tungsten silicide (WS), is then formed. Finally, gate cap layer 58,

comprising SiN or silicon oxide, is formed. The gate conductor layers are then patterned by lithography and dry etched, leaving the gate conductor 59 (comprising gate layer 48, middle layer 56, and gate cap 58) shown in Fig. 12.

[0028] Next, side wall isolation spacers 70, typically comprising silicon nitride, silicon oxide, or a combination of those materials, are created by processes well-known in the art to electrically isolate the wordline (gate conductor 59) from the bitline (the diffusion contact 64). Spacers 70 are typically created by depositing a conformal coating of SiN of about 10 nm to about 100 nm, and performing an anisotropic dry spacer etch process to leave the spacers 70 only on the side walls of gate conductor 59. At this time, optional added implants may be performed to tailor source and drain regions (diffusion regions 62 and 62') of the transistor.

[0029] Next, the isolating regions between multiple gate conductors 59 on the wafer are typically filled with an interlevel dielectric 63, and contact holes are etched via lithography and dry etching to create the holes in which to form diffusion contact 64. Diffusion contact 64 typically comprises doped polysilicon or a tungsten stud. The overlapping region 72 of diffusion contact 64 and of gate cap layer 58 of gate conductor 59, as shown in Fig. 12, is typical of diffusion contacts known as borderless contacts.

[0030] Thus, as shown in Figs. 11A, 11B, and 12, an exemplary trench-side wall array device 60 results from the exemplary process described above. As shown, n+ diffusion regions 62, 62' under diffusion contact 64 adjacent to trench 20 serve as the source and drain of device 60. A channel 66 results in substrate 24 (p-well 50) adjacent faceted side wall 32 of trench 20. Although device 60 as shown in Fig. 11A has been fabricated across the (001) plane, device 60 may also be fabricated across the (011) plane as shown in Fig. 11B. The surface of substrate 24 is typically along the (100) plane. Thus, device 60 may be along a crystallographic plane in the same family as the substrate surface {001}, as shown in Fig. 11A, or may be on a different crystallographic plane (011) in a different family, as shown in Fig. 11B.

[0031] Although illustrated and described herein with reference to certain specific embodiments, the present invention is nevertheless not intended to be limited to the details shown. Rather, various modifications may be made in the details within the scope and range of equivalents of the claims and without departing from the spirit of the invention.

Claims

1. A dynamic random access memory (DRAM) cell including a deep trench storage capacitor comprising:

a side wall defining a trench and being aligned to a first crystallographic plane having a first

crystallographic orientation along a single crystal axis; and

an active transistor device partially disposed on the side wall of the trench.

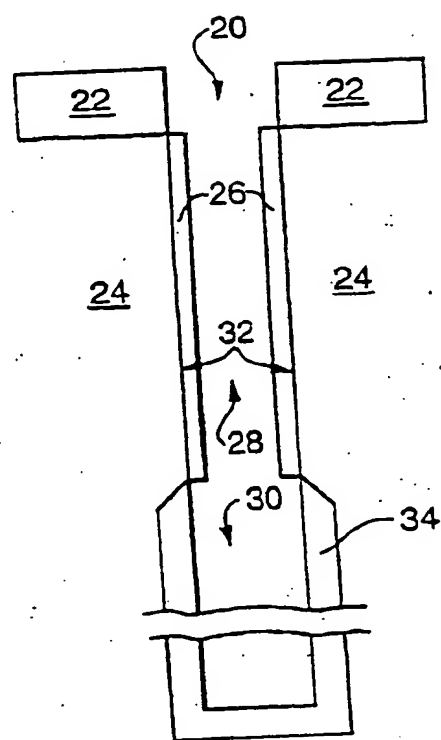
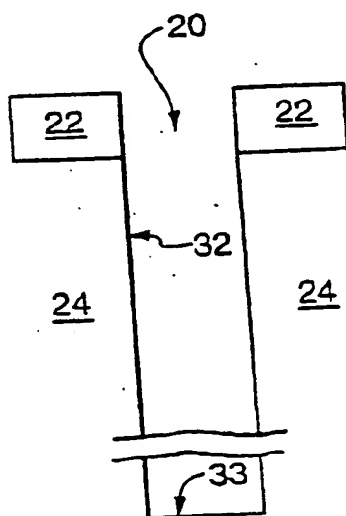
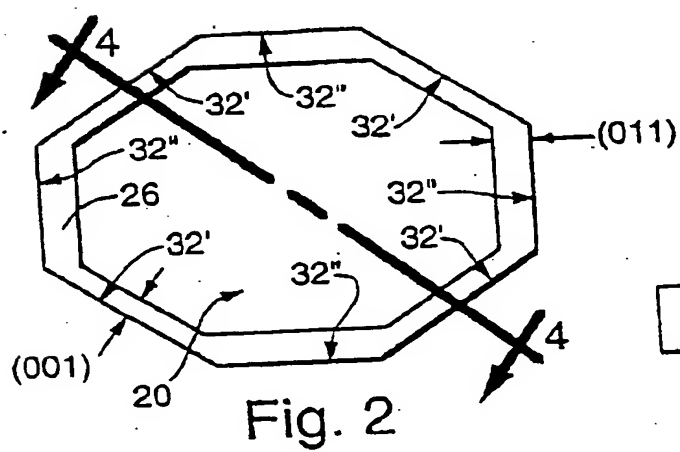
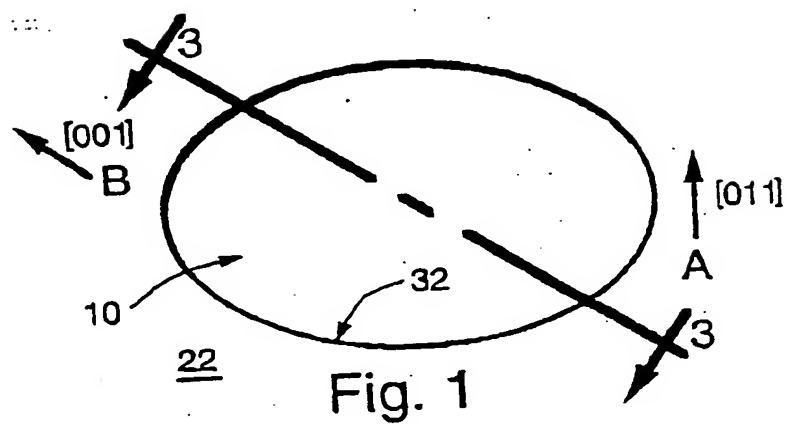
2. The DRAM cell of claim 1 wherein the first crystallographic plane to which the side wall is aligned is (001) silicon.
3. The DRAM cell of claim 1 wherein the first crystallographic plane to which the side wall is aligned is (011) silicon.
4. The DRAM cell of claim 1 wherein the deep trench storage capacitor is located in and on a substrate having a surface extending along a second crystallographic plane, with the first crystallographic plane and the second crystallographic plane in a family of equivalent planes.
5. The DRAM cell of claim 4 wherein the family of equivalent planes is {001} silicon.
6. The DRAM cell of claim 1 wherein the deep trench storage capacitor is located in and on a substrate having a surface extending along a second crystallographic plane, with the first crystallographic plane and the second crystallographic plane in different families of planes.
7. The DRAM cell of claim 6 wherein the first crystallographic plane to which the side wall is aligned is (011) silicon and the second crystallographic plane to which the substrate is aligned is (001) silicon.
8. A process for manufacturing a DRAM cell, the process comprising:
 - (a) forming a deep trench in a substrate, said deep trench having a side wall;
 - (b) forming a faceted crystal region having a single crystallographic orientation along said side wall; and
 - (c) forming a transistor device partially disposed on said faceted crystal region in said side wall.
9. The process of claim 8 further comprising in step (b) forming said faceted crystal region by growing an oxide collar.
10. The process of claim 9 wherein step (b) comprises forming said collar by local thermal oxidation under oxidation conditions selected to promote a higher oxidation rate along a first family of crystallographic

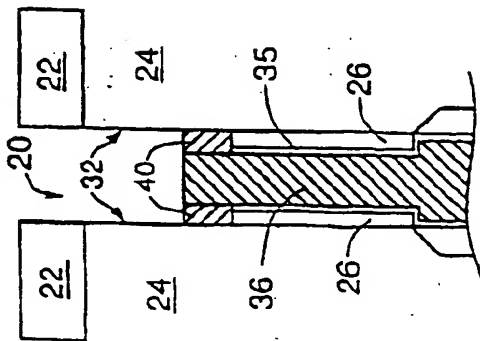
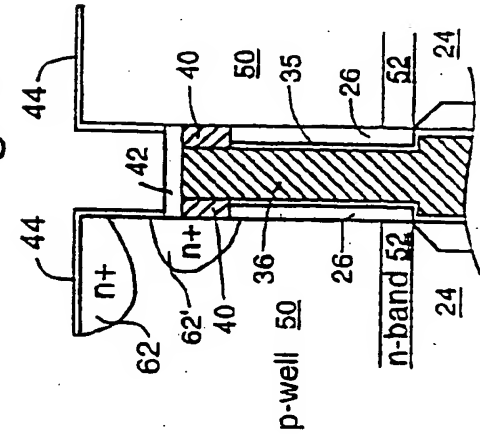
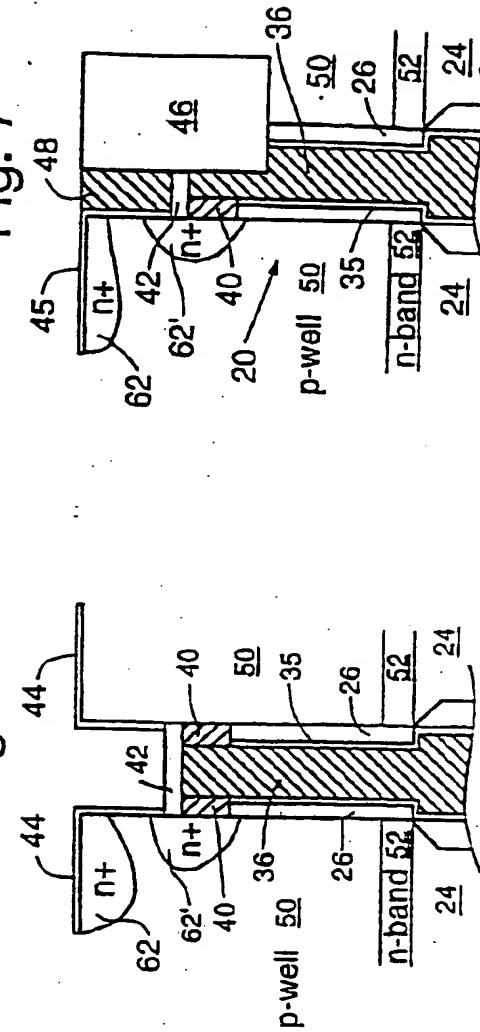
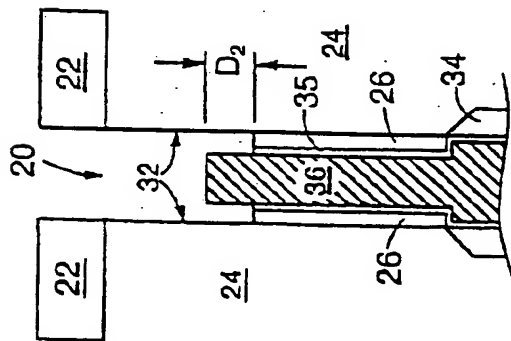
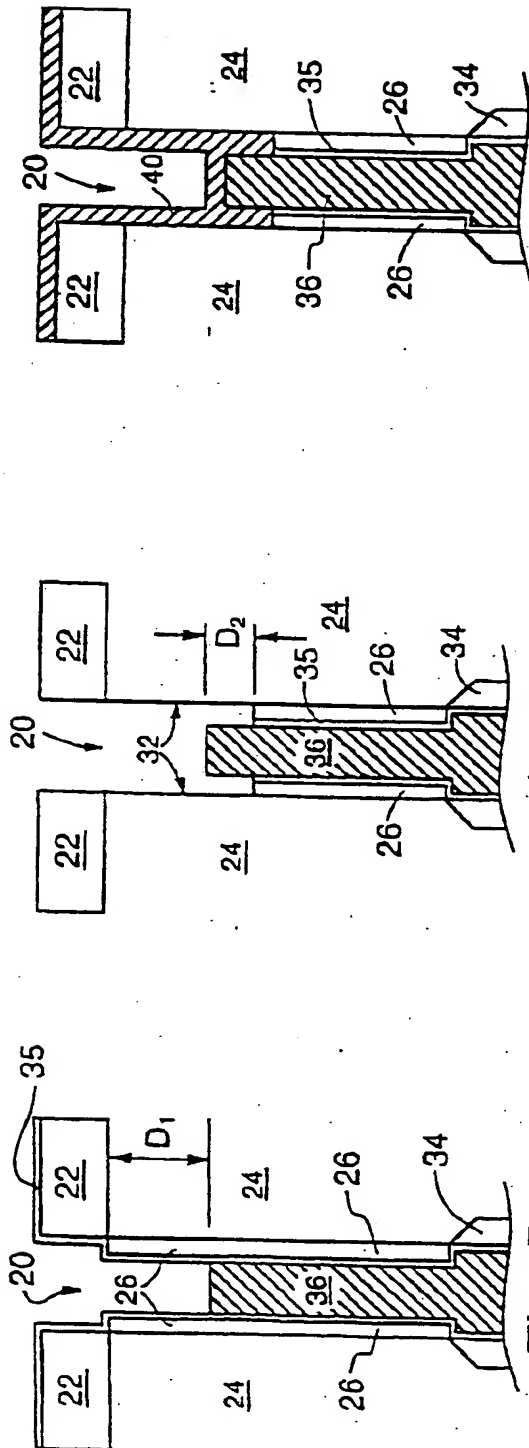
axes than along a second family of crystallographic axes.

11. The process of claim 10 wherein the first family of crystallographic axes is $\langle 011 \rangle$ and the second family of crystallographic axes is $\langle 001 \rangle$. 5
12. The process of claim 11 wherein step (b) comprises locally oxidizing the upper region of the trench with oxygen or water at a temperature of between 800°C and 1,100°C. 10
13. The process of claim 10 wherein prior to the local thermal oxidation step, step (b) further comprises: 15
 - (i) forming a barrier film in the deep trench; and
 - (ii) removing the barrier film from the upper region of the trench. 20
14. The process of claim 13 wherein step (b)(ii) comprises: 25
 - filling the trench with photoresist;
 - partially etching the photoresist into the trench to expose the barrier film in the upper region;
 - removing the exposed barrier film in the upper region by one of chemical and dry etching; and 30
 - stripping the photoresist.
15. The process of claim 8 further comprising in step (b) forming said faceted crystal region by one of a physical and a chemical process. 35
16. The process of claim 15 wherein said chemical process is preferential crystal axis etching. 40
17. The process of claim 16 wherein said chemical process is preferential crystal axis etching with potassium hydroxide. 45
18. The process of claim 8 wherein step (c) further comprises: 50
 - (i) creating a buried plate in the lower region of the deep trench;
 - (ii) partially filling a *region of* said trench with a conductive material; 55
 - (iii) forming a buried strap between an upper part of said filled region and said trench side wall;
 - (iv) forming a trench-top dielectric over said

filled region and said buried strap; and

(v) forming a gate conductor, shallow trench isolation, at least one well, and a diffusion contact





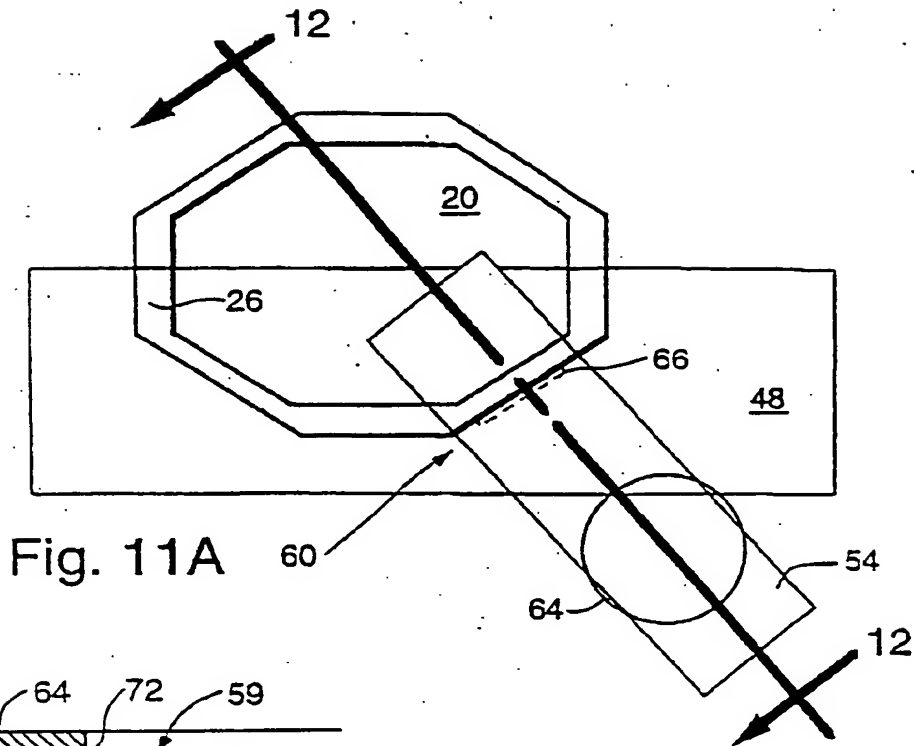


Fig. 11A

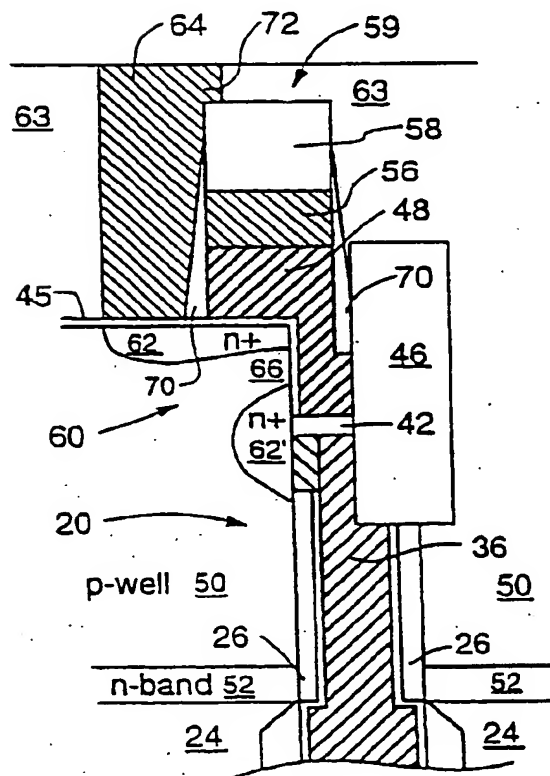


Fig. 12

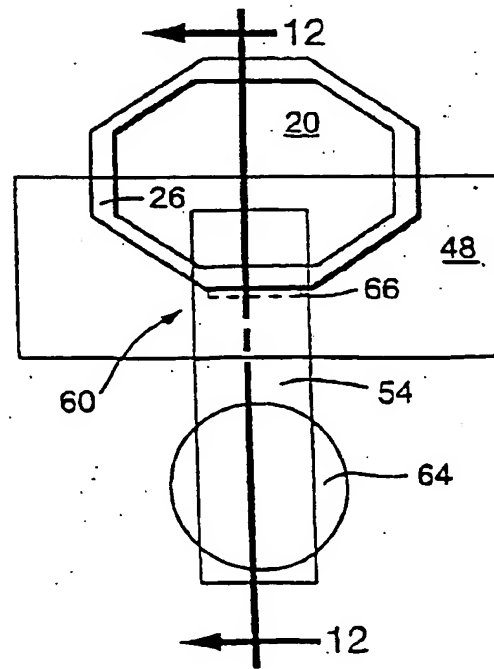


Fig. 11B

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